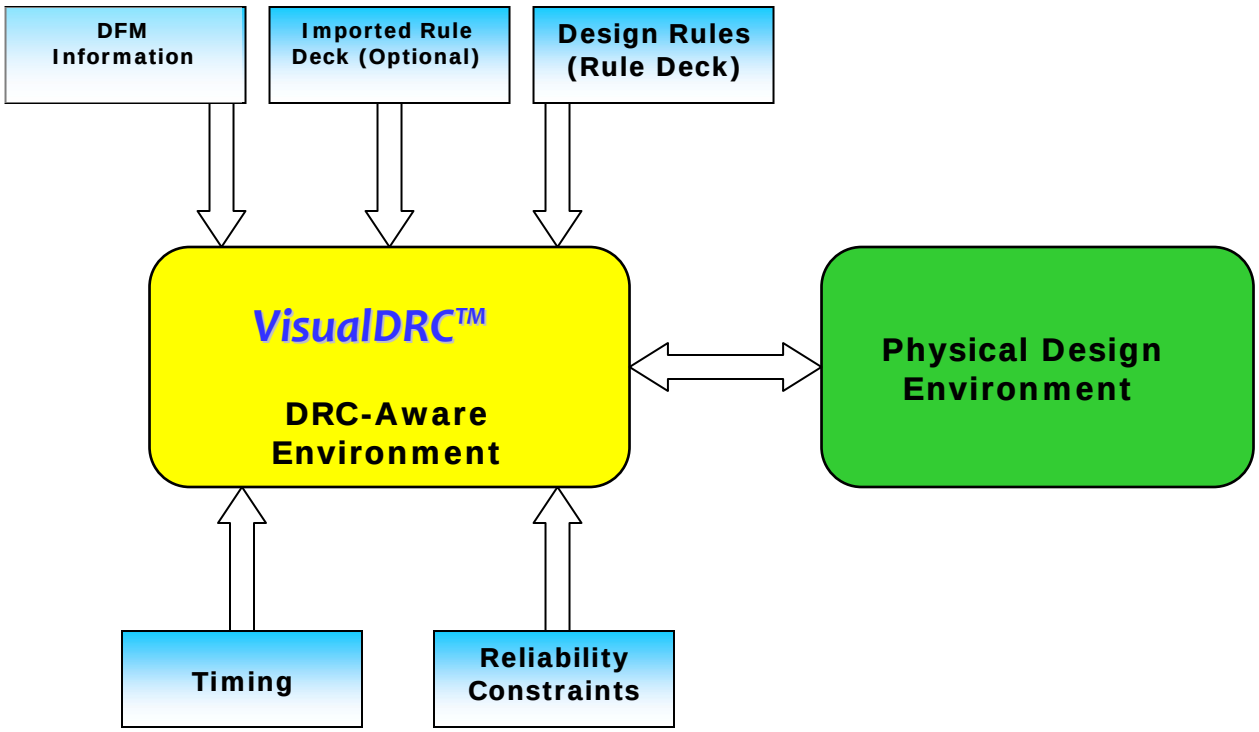
DATASHEET

VisualDRC™

Interactive Design Rule Aware Environment

VisualDRC™ is a Design Rule aware integrated circuit layout design environment. The tool analyzes the IC layout block's database during construction and automatically advises / corrects design rule violations, maintaining the process design rule correctness.

VisualDRC™ provides a real-time DRC-Aware design environment within Cadence's layout editor. (Virtuoso LE, XL, GXL)



VisualDRC™

Interactive Design Rule Aware Environment

VisualDRC™ is an advanced design rule aware environment for mask layout database. ***VisualDRC™*** is aimed for fast, accurate, and efficient design rule violation analysis and elimination during the construction of a mask layout database with ease. ***VisualDRC™*** reads its own proprietary rule deck or imported industry standard run sets which describe the process design rule and constraints. Then the tool performs an on-the-fly design rule analysis of the constructed layout and advises about existing or created violations. ***VisualDRC™*** has the capability to automatically correct these violations, maintaining the process's design rule accuracy.

Benefits

Significantly reduces design rule verification time - During the construction of a mask layout block, ***VisualDRC™*** reads the built-in layout editor's database, analyzes for process design rule violations and provides interactive suggestions and alternative corrections according to current polygons status. Each suggestion and alternative correction is accompanied with full detailed report about the found violation.

VisualDRC™ **-** Innovative EDA program which is based on recent real-time technology. This program is a plug-in into Cadence's Virtuoso platform, enabling the interactive DRC (Design Rule Check) and correction environment. The program can read an external industry standard rule deck (Calibre, Hercules, Assura) and automatically alerts about design rule violations during the construction of an IC layout block.

VisualDRC™ provides you with a clear and immediate graphical representation of your design's design rule analysis, before and after correction.

VisualDRC™ Compatible with UNIX and Linux platforms.

VisualDRC™ interfaces with Cadence's Virtuoso via SKILL and OpenAccess. In addition, the system offers key function access via API calls for customization and personalization purposes.

VisualDRC™ fully supports OpenAccess for future interoperability and enhancements. In order to ensure versatility, our tool fully supports OpenAccess enabling interaction with industry's standard scripting languages, providing full customization possibilities.

Features

VisualDRC™ - A new approach in integrated circuit design rule verification methodology. Our software provides an advanced approach in order to easily analyze each design rule violation and provide an immediate correction.

VisualDRC™ works in flat and/or Hierarchical mode. In flat mode ***VisualDRC™*** detects design rule violations at the current edited level only. In hierarchical mode the tool checks for topological correctness through all block levels.

The main advantage of this concept is the creation of a Design Rule-Aware IC layout design environment that eliminates ahead of time process rules violations that may consume significant DRC verification time later in the design flow.

The system provides a powerful tool to eliminate design rule violations during the construction of IC layout block, considering the entire block's hierarchy.

VisualDRC™ **- Advise Mode** allowing the user to work in a non-invasive manner detecting design rule problems during the construction of a mask layout block and recommending alternative options for correction.

VisualDRC™ **- Auto Correct Mode -** This mode provides automatic correction of design rule violations in a layout block. The tool analyzes the layout block and automatically corrects all layout topological violations, maintaining the process design rule accuracy.

VisualDRC™ **-** Information Window - Quick description fields enable users to get all desired details about any design rule violation and its suggested correction. The Information Window enables users to quickly assess the nature of the design rule issue and provide vital information about current and suggested correction.

VisualWinCheck™ **-** Window Check and Correction: User has the capability to check for design rule violations within a selected window. The system performs fast design rule verification within the selected window and graphically presents the violations. (if exist) In addition the system offers possible solutions. The user may accept or reject the suggested solutions according to desire.

VisualDRC™ **-** The system provides Full nanometer support, including deep nanometer ranges.
(65nm, 45nm, 32nm)

VisualDRC™ **-** Advanced viewing system provides an accurate graphical representation of design rule violations within the Virtuoso design environment. (Violation Browser)

VisualDRC™ **-** Universal & Fully Customizable. Users can customize and personalize their options.

VisualDRC™ **-** Supports digital. Analog and mixed signal designs.

Specifications

- ✓ Interactive Design Rule Aware environment for mask layout database.
- ✓ The tool reads its own property rule deck for process design rules.
- ✓ The tool imports industry standard design rule run sets files. (Calibre, Hercules, Assura)
- ✓ Advanced viewing system provides real-time graphical representation of design rule violations.
- ✓ **Advise** mode to guide users about potential design rule violations during the construction of an IC's mask layout database and suggested solution.
- ✓ **Auto-Correct** mode to automatically correct design rule violations during the construction of an IC's layout database, maintaining process design rules!
- ✓ Flat and fully Hierarchical analysis.
- ✓ Suggests few alternative design rule correction options. The user has the choice of selecting the best option in order to eliminate design rule violation providing the highest quality.
- ✓ Quick description fields provide comprehensive information about found design rule problems and suggested methods for correction.
- ✓ ***VisualWinCheck™*** allows selective window area design rule check and correction.
- ✓ Advanced graphical setup for easy identification of potential design rule violations.
- ✓ Full nanometer support, including deep nanometer ranges.
- ✓ Universal & Fully Customizable. Users can customize and personalize his/her analysis/correction options including internal macro language for in-house enhancements.
- ✓ OpenAccess support further contributes to open interoperability and ensures ease of tool integration for customers.
- ✓ Exclusively developed for Cadence's Virtuoso platform. (Virtuoso LE/XL/GXL)
- ✓ Exporting & importing of design parameters from related Cadence tools and environments in order to provide all necessary analysis and auto-correction information. (DFM Constraints)
- ✓ Supports all design types, including digital, analog and mixed signal.

Design Inputs

- All Cadences' Virtuoso supported formats (Layout database)
- Property rule deck for process design rules information. (Built-in UMC, TSMS nanometer rules support. 90, 65, 45nm)
- Importing industry standard design rule run sets (Calibre, Hercules, Assura)
- Timing constraints to maintain timing information for sensitive nets.
- Reliability constrains to prevent Electromigration and Self Heat violations.
- DFM constrains support (OPC, PSM, Litho)

Design Outputs

- Graphical representation of potential & existing design rule violations
- Design rule violations analysis reports
- Full Correction of mask layout database (Auto-Correct Mode)

Platforms/OS

- Sun/Solaris
- Linux

Third-Party Support

- Open Access tools and functions

Services and Technical Support

- ✓ We are committed to ensure customer-focused solutions that increase ROI, reduce risks, and achieve design goals faster!
- ✓ Proven methodology and flow tuned to your design environment.
- ✓ Professional applications engineers provide technical assistance to ensure efficiency and high productivity!
- ✓ Product and flow training to fit your needs and preferred learning style
- ✓ Efficient customer support that keeps your design team productive!
- ✓ Online support gives you access to software updates, technical documentation, and more - 24 hours a day, 7 days a week.

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